a reference phase accumulator operational to accumulate a frequency division ration command and a modulating data signal and to generate an accumulated frequency control word (FCW) therefrom;

a phase detector operational to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a phase error in response thereto;

a loop gain alpha multiplier element operational to generate the loop gain alpha multiplier signal in response to a filtered direct modulator output signal; and

a direct modulator operational in response to the modulating data signal and the filtered phase error to generate the filtered direct modulator output signal.

2. (amended) The digital phase-domain phase-locked loop circuit according to claim 1 wherein the direct modulator comprises:

a loop gain alpha inverse multiplier element operational to generate a signal in response to the modulating data signal; and

a combinational element feeding the loop gain alpha multiplier element in response to the signal generated by the loop gain alpha inverse multiplier element and further in response to the phase error.

4. (amended) The digital phase-domain phase-locked loop circuit according to claim 1 further comprising an all-pass filter operational to pass a phase error generated via the phase detector to generate the phase error.

6. (amended) A digital phase-domain phase-locked loop circuit comprising:

a digitally-controlled oscillator (DCO);

a gain element feeding the DCO and operational to compensate for DCO gain in response to a direct modulator output signal;

an oscillator phase accumulator operational to accumulate DCO generated clock edges;

a reference phase accumulator operational to accumulate a frequency control word (FCW) therefrom;

a phase detector operation to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a phase error in response thereto;

a loop gain alpha multiplier element operational to generate a loop gain alpha multiplier signal in response to the phase error; and

a direct modulator operational in response to the modulating data signal and the alpha multiplier signal to generate the direct modulator output signal.

9. (amended) The digital phase-domain phase-locked loop circuit according to claim 6 further comprising an all-pass filter operational to pass said phase error generated via the phase detector to generate a filtered phase error.

11. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the phase error.

12. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock, the digitally-controlled oscillator comprising a voltage controlled oscillator; and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

13. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW, said direct modulator comprising a combinational element feeding the digitally controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

14. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW;

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error; and

a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL.

17. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error, said PLL comprising a phase detector feeding an all-pass filter, wherein the phase detector is responsive to the channel selection signal operational to pass the phase error to generate a filtered phase error.

Please add the following new claims:

22. The digital phase-domain phase-locked loop circuit according to claim 1 wherein said phase error is a filtered phase error.

23. The digital phase-domain phase-locked loop circuit according to claim 6 wherein said phase error is a filtered phase error.

24. The phase-locked loop system according to claim 11 wherein said phase error is a filtered phase error.

25. A method of operating a digital phase-locked loop (PLL) comprising the steps of:

providing a phase-locked loop including a digitally-controlled oscillator (DCO) having a gain K_{DCO}, and a phase detector, wherein the DCO is responsive to an oscillator tuning word (OTW) to generate a DCO output clock having a frequency fv, and further wherein the phase detector is responsive to a channel selection signal, a modulating data signal and the output clock to generate a phase error;

providing a direct modulator operational in response to the phase error and the modulating data signal to generate the OTW;

observing an accumulated phase $\Delta\emptyset$ in the phase error in response to a given change Δx in the OTW; and

estimating the DCO gain such that a DCO gain can be compensated to substantially remove its effects on loop behavior.

REMARKS

Claims 1-10 and 18-21 stand allowed. By this amendment Applicants amend the term

claim 18 uses the term "phase error" without the filter limitation.